Approvals:

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Revision History

Date	Change / ECO Notice	Change Description
04/24/2014	A	Initial Draft
06/05/2020	12586	Updated equipment board sizes and component spacing, added DWI-009-002-48 under References. Changed the doc # from DQP-022-003 to DQP-041.
4/27/2021	13539	Change 3.1 to updated form number. Inserted sections 6.28 and 6.29 for test.
3/24/2025	17368	Wording and in section 6.28 has been updated to match current flying probe specs.

1.0 Purpose:

1.1 To define the methods utilized for reviewing the manufacturability of new designs to insure potential issues are resolved before the initial build which will save time and improve product quality.

2.0 Scope:

2.1 This procedure is applicable to all new assemblies manufactured at Distron.

3.0 Applicable Documents:

3.1 New Product Risk Mitigation Analysis (DF-024-004)

3.2 PCB Fiducial and General Mfg Requirements Procedure (DWI-009-002-48)

4.0 Definitions:

4.1 PCB – Printed Circuit Board

4.2 SMD – Surface Mount Device

4.3 BGA – Ball Grid Array

5.0 Responsibilities:

5.1 It is the responsibility of the Manufacturing and Management Representatives and/or designee to ensure the requirements within this procedure are followed and for training applicable personnel.

5.2 It is the responsibility of the Engineering Department to ensure all new designs are reviewed per this procedure.

6.0 Procedure:

6.1 **Fiducials:**

6.1.1 Distron's automated equipment utilizes fiducials as reference points that are required for accurate assembly of components on PCBs.

6.1.2 Fiducials are an artwork feature created within the PCB conductive pattern to provide a measureable point for component mounting and are utilized by the automated equipment's imaging system as a point of reference to locate a position of all PCB land patterns.

6.1.3 Fiducials are placed on the top and bottom copper layer. They should not be placed on the mask or silkscreen layer because the layers are not as precise as the copper layer.

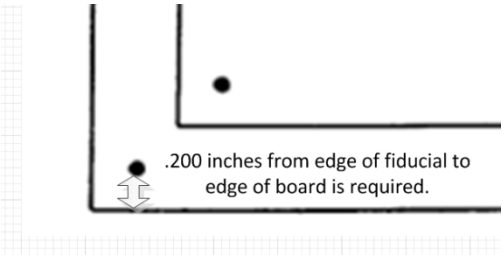
6.1.4 Board fiducials are used to locate the position of all PCB land patterns.

6.1.5 Panel Fiducials are used to locate the rails or perimeter of a multi-up panel.

6.1.6 Board and panel fiducials are required.

6.1.7 Fiducial spacing is from the edge of the board to the edge of the fiducial and must be at least .200 inches as shown below.

Note: Reference the PCB Fiducial and General Mfg Requirements Procedure (DWI-009-002-48) for additional information.



6.2 **Board Sizes:**

The table below lists the minimum and maximum board sizes that will fit Distron's assembly equipment.

Through Hole Equipment Board Sizes

Equipment	Min. Length and Width board size (inches	Max. Length and Width board size
Electrovert Wave Solder Machine	2" width	16" conveyor width /14" soldering width
Pillarhouse Selective Solder Machine	4"x4"	20"x18"
Juki Selective Solder Machine	.79"x .79"	18"x18"

SMT Equipment Board Sizes

Equipment	Min. Length and Width board size (inches)*	Max. Length and Width board size (inches)*
Dek 03iX Screen Printers	1.96"x1.59"	20"x20"
Vitech Pi Paste Inspection Equipment	2"x2"	21"x21"
Mycronic Pick and Place Equipment	2.7"x2"	22"x20"
Heller 1809 Reflow Ovens	2" (width)	18"-20" (width)
Yestech AOI Inspection Equipment	2"x2"	22"x20"
Vitech 3D AOI Inspection Equipment	2"x2"	21"x24"
Dage XRAY Equipment	na	29"x22"/inspect area 20"x17.5"

*Minimum and maximum board size may be affected by stand-alone or in-line configuration.

6.3 **Polarity Marks:**

All polarized parts should have polarity marks that are in the silkscreen layer or the copper layer. The marks should be visible after the components are installed for inspection purposes.

6.4 **Diode Orientation**

6.4.1 Clearly identify the orientation of the various types of diodes.

6.4.2 It is preferred to use a "C" for cathode side or "A" for anode side or use the schematic diode symbol.

6.4.3 Ensure the diode marks are visible after installing the components.

6.5 **Lead to Hole Ratio:**

6.5.1 **Through Hole Components:**

6.5.1.1 Adequate space within the hole is required to ensure the proper vertical fill of solder and for automated insertion.

6.5.1.2 The finished hole size should be .019” larger than (>) the diameter of the lead.

6.5.1.3 The diameter for square leads would be the distance across diagonal corners of the lead.

6.6 **Tabs/Mousebites:**

6.6.1 Tabs are used to connect PCBs within a routed panel.

6.6.2 Mouse bites are the holes within the tabs that allow the board to be cleanly broken out of the panel.

6.6.3 General guidelines:

6.6.3.1 For an .063” thick PCB, utilize .050” wide tabs placed every 2 inches with a .018” hole placed within the center of PCB edge at .028” pitch.

6.6.3.2 Larger and thicker boards will require wider tabs.

6.6.3.3 Internal copper will need to be relieved from the PCB edge.

6.6.3.4 Keep traces away from the mouse bite holes to prevent any damage during separation.

6.6.3.5 For tab routed areas on panels, the opening size should be .080" wide x .450" in length to allow for a nibbler tool to cut each board out of the panel

6.6.4 Distron can assist with panel design if needed to ensure the process is optimized.

6.7 **Panel Breakaways:**

6.7.1 Panel breakaways may interfere with overhanging components.

6.7.2 Panel design should allow for connectors that overhang the board edge.

6.7.3 Tabs/mouse bites should not be placed under the connectors to prevent potential damage during depenalization.

6.7.4 Keep-out areas may need to be designated within the Gerber files so the tabs and mouse bites are not located under a connector or near a trace close to the edge of the PCB.

Note: This information is also helpful when V-scoring is used.

6.8 **Components Too Close to the PCB Edge:**

6.8.1 Manufacturing equipment clamping mechanisms require un-obstructed room to grab the PCB effectively.

6.8.2 Delicate components, such as ceramic capacitors and resistors, are at risk of cracking when they are placed too close to the edge.

6.8.3 Components should be placed 6.35 mm from the PCB edge.

Note: Parallel to the PCB edge is better to prevent potential damage during depanelization.

6.9 **Cleaning:**

6.9.1 Aqueous cleaning is used to remove water-soluble fluxes after soldering. Sealed components are preferred or utilize a No Clean Soldering process for the entire assembly.

Note: Some unsealed components are not able to withstand the aqueous cleaning process. For example, switches, speakers, batteries and buzzers may not be compatible with this cleaning process.

6.9.2 Components that are not compatible with cleaning may require manual soldering which increases cost.

6.9.3 The assembly drawing should note any components that cannot be washed such as unsealed components.

6.9.4 Some components are required to be baked after wash to remove any residual moisture trapped inside, as specified by the customer.

6.10 **Vias:**

6.10.1 Vias in pads can drain solder away from the component solder joint and create an insufficient joint. There is also potential that a visual inspection may miss the insufficient joints. Avoid vias in pads if possible.

6.10.2 Allow a .015” of solder mask if utilizing solder mask to separate the via from the pad.

6.10.3 Filled vias may also be used to prevent solder drain.

6.10.4 Avoid unmasked vias under BGAs. IPC recommends uniform Solder Ball Terminations for BGAs which may not be achievable with unmasked Vias.

6.10.5 Masked vias under BGAs are preferred. Avoid using different size solder pads for BGAs so that uniform solder ball terminations will be achieved.

6.10.6 Unused vias on the solder side should be covered with solder mask to reduce the risk of solder bridging.

6.11 **Solder Mask:**

6.11.1 Solder Mask between fine pitch pads is recommended to reduce solder bridges.

Some PCB fabricators require at least a .004” wide to fit the solder resist. Therefore, it may be best to check with the PCB fabricator on their requirements.

6.11.2 Solder mask between pads of passive components can contribute to drawbridge defects and flux entrapment.

Therefore, it is recommended to remove the Solder Mask between the pads of the passive components and when there are no traces between the pads.

6.12 **NSMD or SMD pads for BGAs**

Non Solder Mask Defined (NSMD) pads are preferred in order to have uniform sized solder joints on BGAs.

6.13 **Lead Free Solder Balls on BGAs in a Leaded design:**

Notify Distron if Lead Free devices will be utilized on a Tin Lead design.

Note: Reflow profile adjustments will be needed.

6.14 **Thermal Relief:**

6.14.1 Solder up flow on through hole components is required to meet IPC requirements.

6.14.2 Thermal relief improves the ability to reach the temperature to get adequate solder up flow on through hole parts; especially on heavy Copper planes and boards with large thermal mass.

6.14.3 Ensure adequate thermal reliefs exist on the design.

6.15 **Wire Modifications:**

Wire modifications are usually labor intensive. It may be more reliable and less costly to design the change into the PCB.

6.16 **BGA Component Spacing:**

A .150" spacing is recommended around BGAs to allow enough room for hot air rework tools if upgrades or replacement is required.

6.17 **Selective Soldering Spacing:**

A .1" spacing is preferred between through-hole lead and SMT components.

6.18 **No Clean Solder & Flux Residue:**

6.18.1 No Clean solder chemistry is recommended on some components such as QFNs, micro BGAs and LGAs because of the difficulty in removing water soluble flux under the components.

6.18.2 Flux residue may affect high impedance designs.

6.18.3 Ensure flux residue after manufacturing is acceptable if utilizing No Clean chemistry.

6.18.4 Ensure the preferred solder chemistry is identified.

6.19 **Trace Cuts:**

It may be more cost effective to revise the board and change the PCB rather than requiring trace cuts since it is a manual process.

6.20 **SMT vs Through-Hole:**

6.20.1 Distron recommends SMT components wherever possible. Through-hole assembly steps will add cost to the assembly.

6.20.2 Investigate if there are SMT alternatives if a design has a few through-hole parts for potential cost savings.

6.21 **Lead Lengths of Through-Hole Components:**

6.21.1 Identify any special lead length requirements or other component height requirements.

6.21.2 Lead length requirements below .040" add labor cost.

6.21.3 Lead length requirements above .15" or 4.00mm add labor cost.

6.22 **PCB Finish**

Electroless Nickel Immersion Gold per IPC-4552 is the preferred finish as it provides flat pads and has a long storage life.

6.23 **PCB Fabrication**

6.23.1 Define the laminate stack up clearly.

6.23.2 Determine which board fabricator is capable of building the board based on the following characteristics:

- Minimum trace width
- Minimum distance between traces
- Smallest hole diameter

6.24 **Workmanship Class:**

Identify the assembly workmanship class (Class 1,2 or 3) and any other build standards required on assembly documentation.

6.25 **PCB Laminate Specification:**

6.25.1 Identify the PCB laminate material specifications in the PCB fabrication drawing.

6.25.2 For Lead Free/ROHS assemblies, the laminate must have a glass transition temperature (Tg) of greater than or equal to (≥) 175°C.

6.26 **Labelling and Traceability**

6.26.1 Identify product labelling and traceability requirements on assembly documentation.

6.26.2 It is recommended to include an outline box in the silkscreen layer for the label.

6.27 **Torque Specifications:**

Identify torque requirements in assembly documentation.

6.28 **Probe and Fixture Guidelines:**

- Test Pads/Vias on all Nets.
- Index Tolerance + 0.002 inches Datum to Test Pad.
- Two Tooling Holes on UUT + 0.002 Tolerance between them.
- Tooling Hole Diameters + 0.0031 / -0.000 inches.
- Test Pad / Via Pad Size 0.035 to 0.040 inches.
- Test Pad / Via Pad Separation 0.015 inches.
- Test Pad Center to Center Spacing.

Priority	Preferred	Acceptable
1	0.100”	0.085”
2	0.075”	0.070”
3	0.050”	0.050”

- Test Pads can be located on both sides of board.
- Keep Component Height on test side less than 1.0” if possible.
- No components or test pads closer than 0.125” from edge of UUT.
- No resist on test pads.
- Fill through hole vias with solder
- No probing of component leads.
- Distribute test pads evenly over PC Board.
- Provide clearance space for fixture push finger.
- Minimize fixture changes when redesigning boards

6.29 **Electrical Design Guidelines:**

- Provide Test Access to All Electrical Nodes.
- Place Test Pads as close as possible to signal source.
- Include 2 Test Pads on each Electrical Node tied to Critical Low Impedance.
- **DO NOT** rely on edge connector, circuit traces, or SMT Device Pads for Test Points.
- Use pull up and fill down resistors for control of IC Control Lines.
- Include Test Pads for unused Device Pins.
- Includes method to disable Clock Sources.
- Provide Disable methods for ALL Programmable Logic Devices.
- Include Pull-up loads on all open device inputs.
- Provide disable methods for all Bussed Devices, High Current Devices, and Devices tied to Flash, Rams, EEProms, and D/A Converter.
- Include – circuitry to Disable Feedback Loops.
- Use Devices with short Initialization Times.
- Provide Vectors for all ASIC and Custom Devices
- In using Vectorless test don't use devices with heat sink or ground plans on top.
- Supply Documentation for Device Logic Function.
- Use IEEE 1149 Boundary Scan and 1149.4 Analog and Mixed Signal compatible devices.
- Isolate Power – On Reset Circuits from other digital devices.
- Place Test Pads and Power and Ground Nodes as close as possible to each Digital Devices under test.
- Use multiple test pads on power and ground connections.
- Allow for Battery Isolation during In-Circuit Test.
- Buffer Test Pads to Analog and Mixed Signal Devices.
- Keep In-Circuit Testing in mind when implementing Engineering Changes.

6.30 **Regulatory Requirements:**

Identify all regulatory requirements.

6.31 **Packaging Requirements:**

Identify any special final packaging requirements.

6.32 **Design Checklist**

Utilize the New Product Risk Mitigation Analysis (DF-024-004) to confirm the assembly is manufacturable which will ensure a robust manufacturing process and product reliability.

7.0 Records:

7.1 Keep records per the Records Control Procedure (DQP-016).

End of Document